



1/16

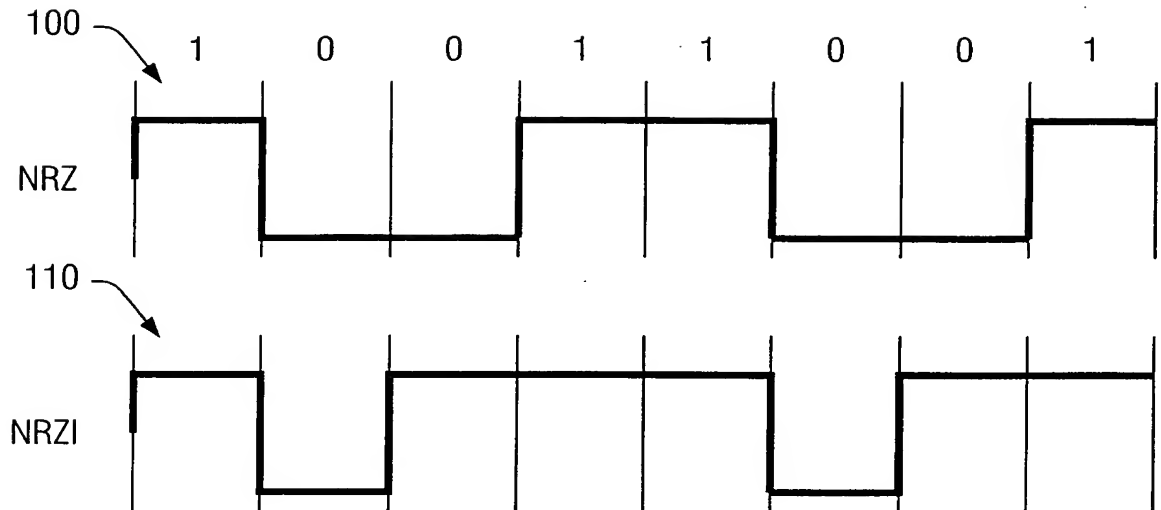


FIG. 1
PRIOR ART

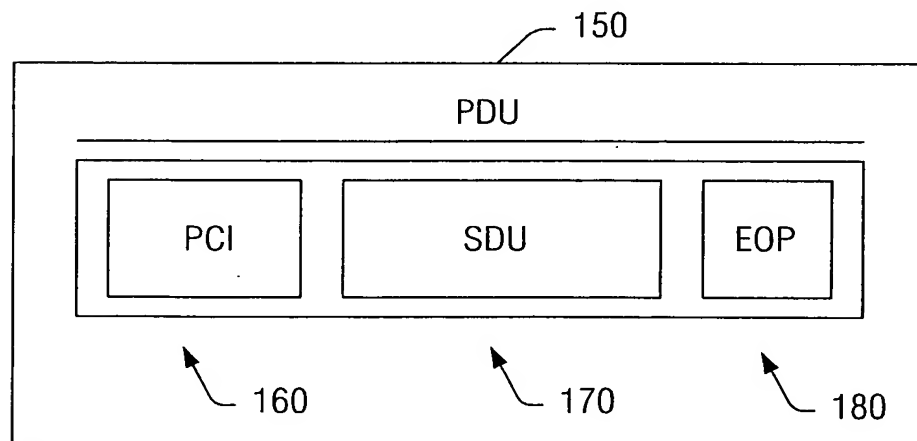


FIG. 2
PRIOR ART

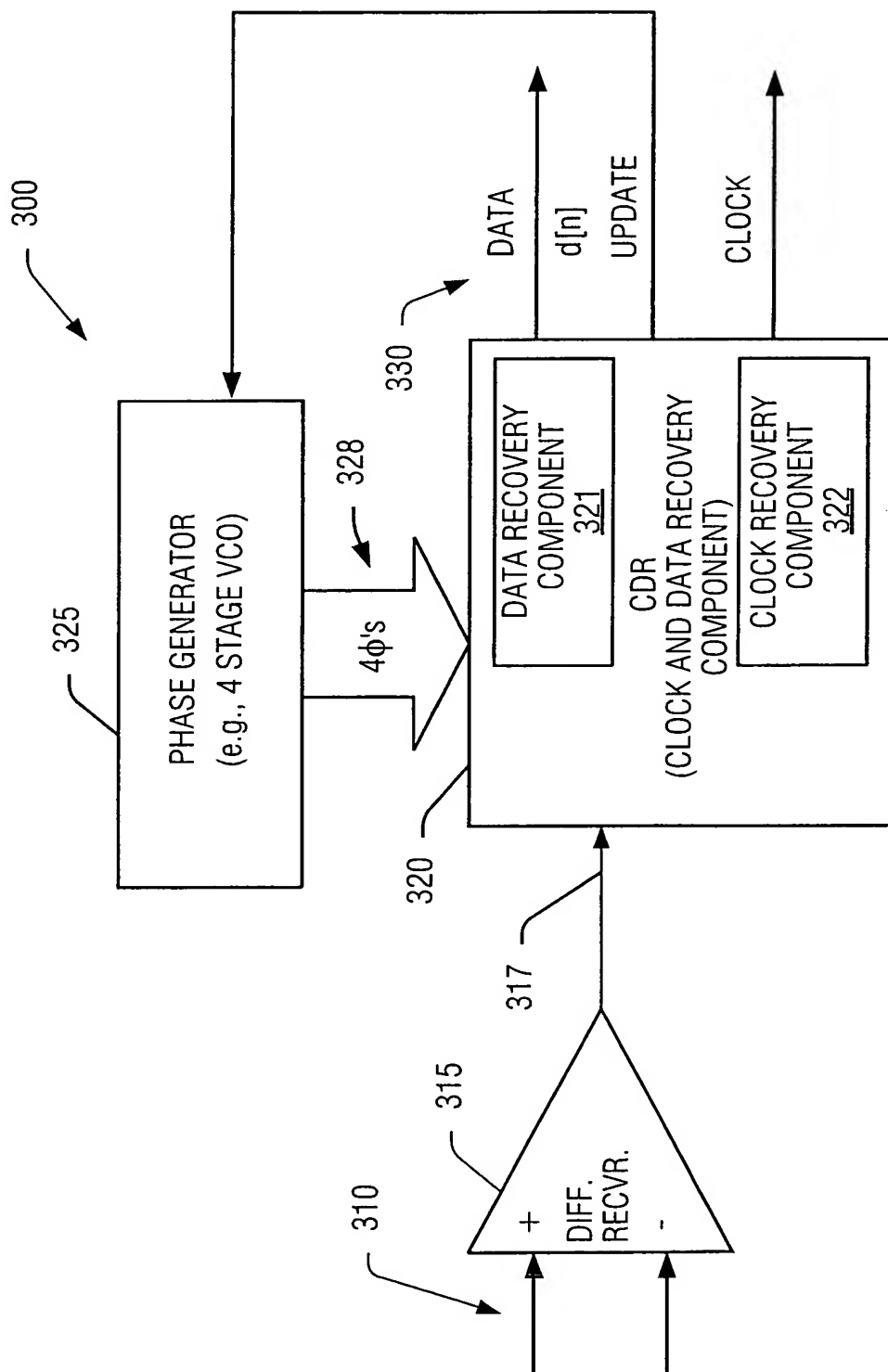


FIG. 3A

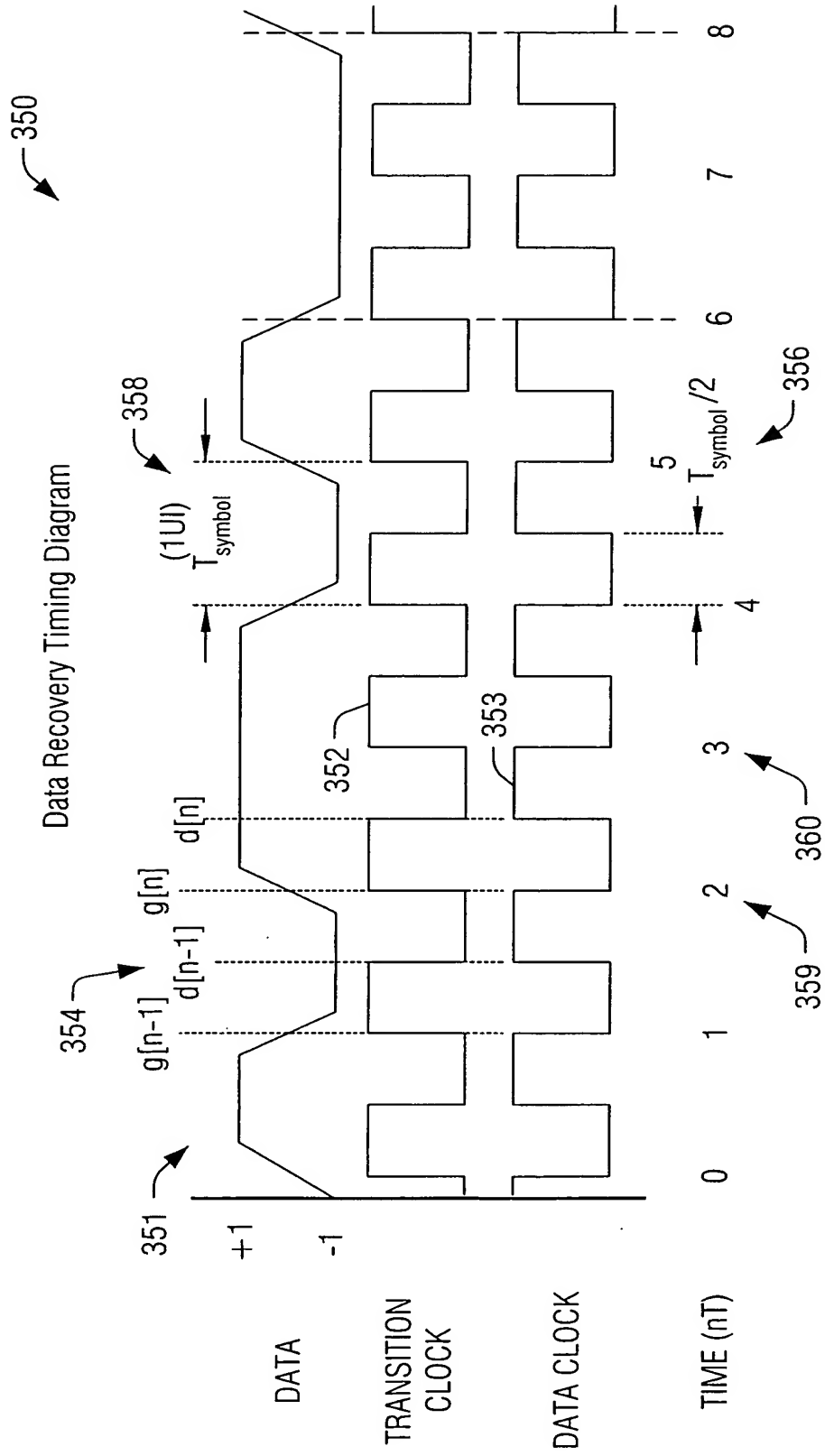


FIG.3B

4/16

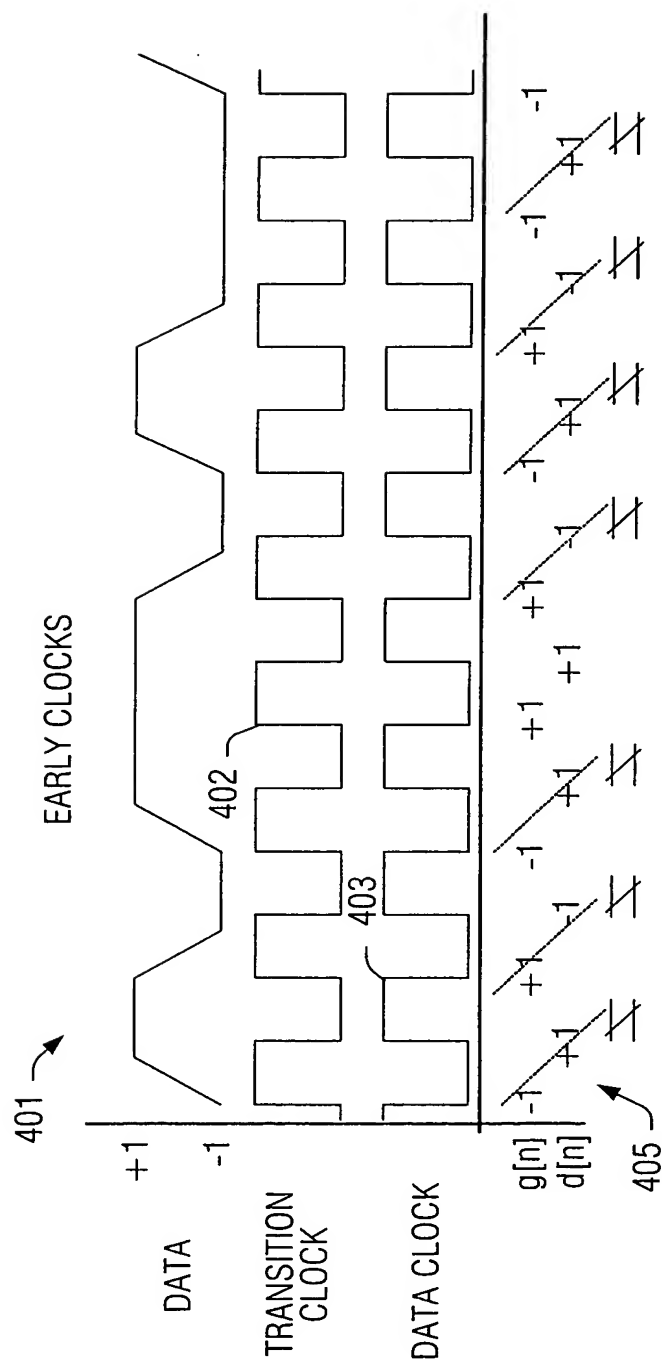


FIG. 4

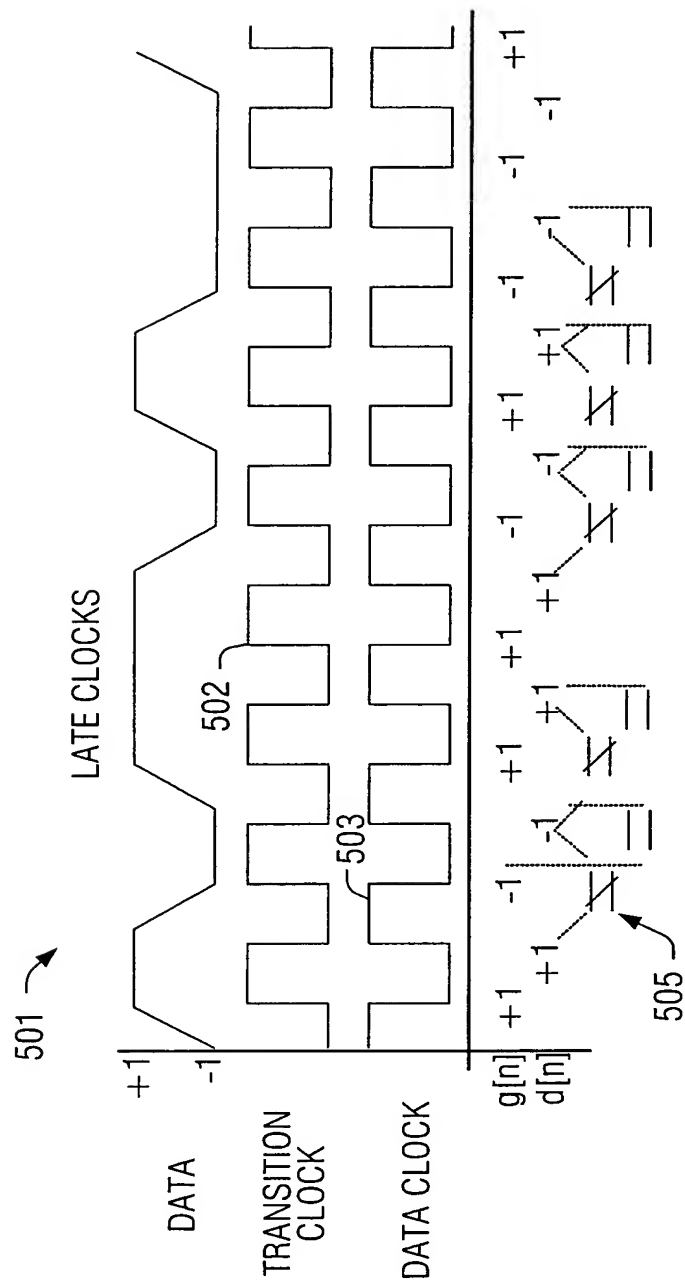


FIG. 5

6/16

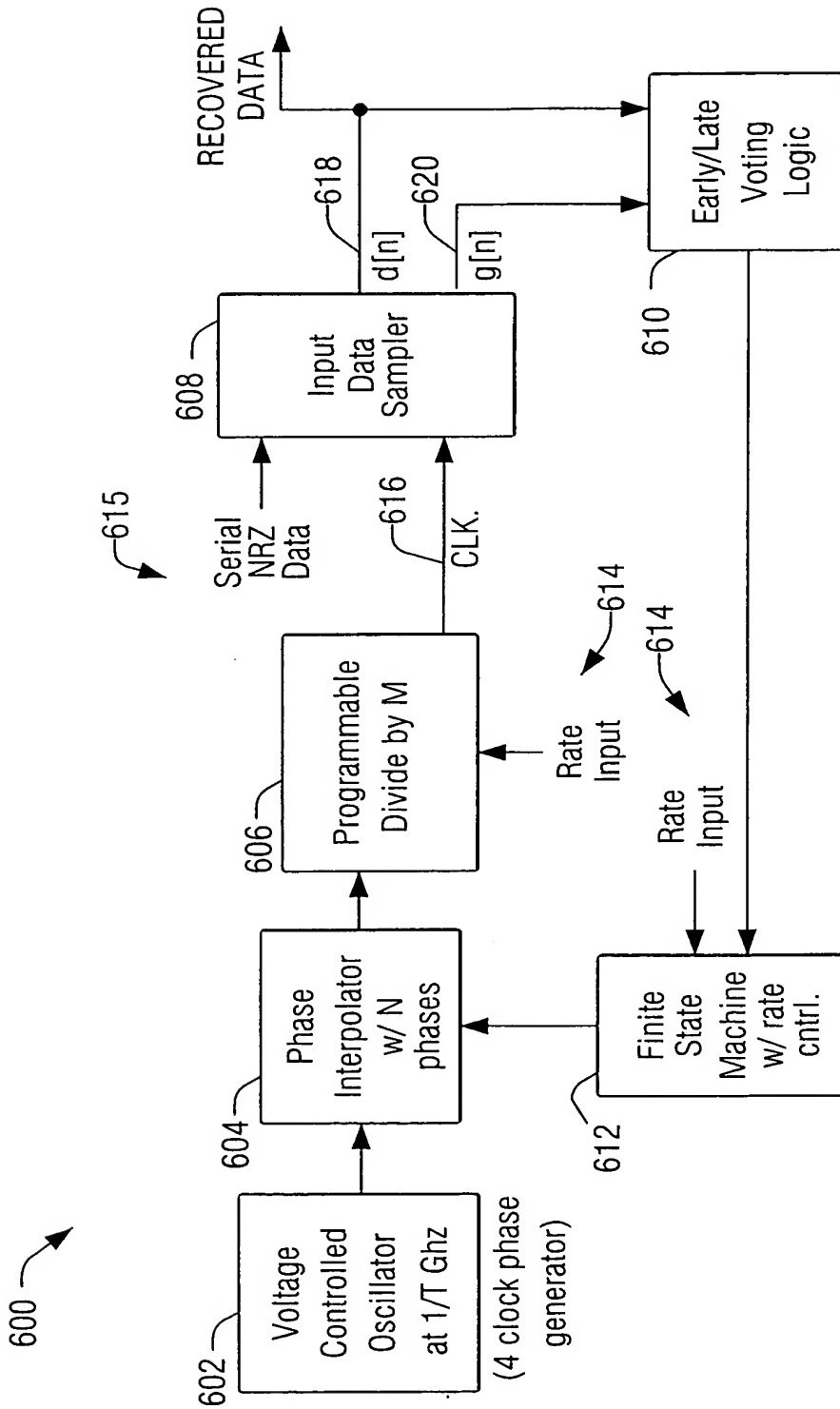


FIG. 6A

7/16

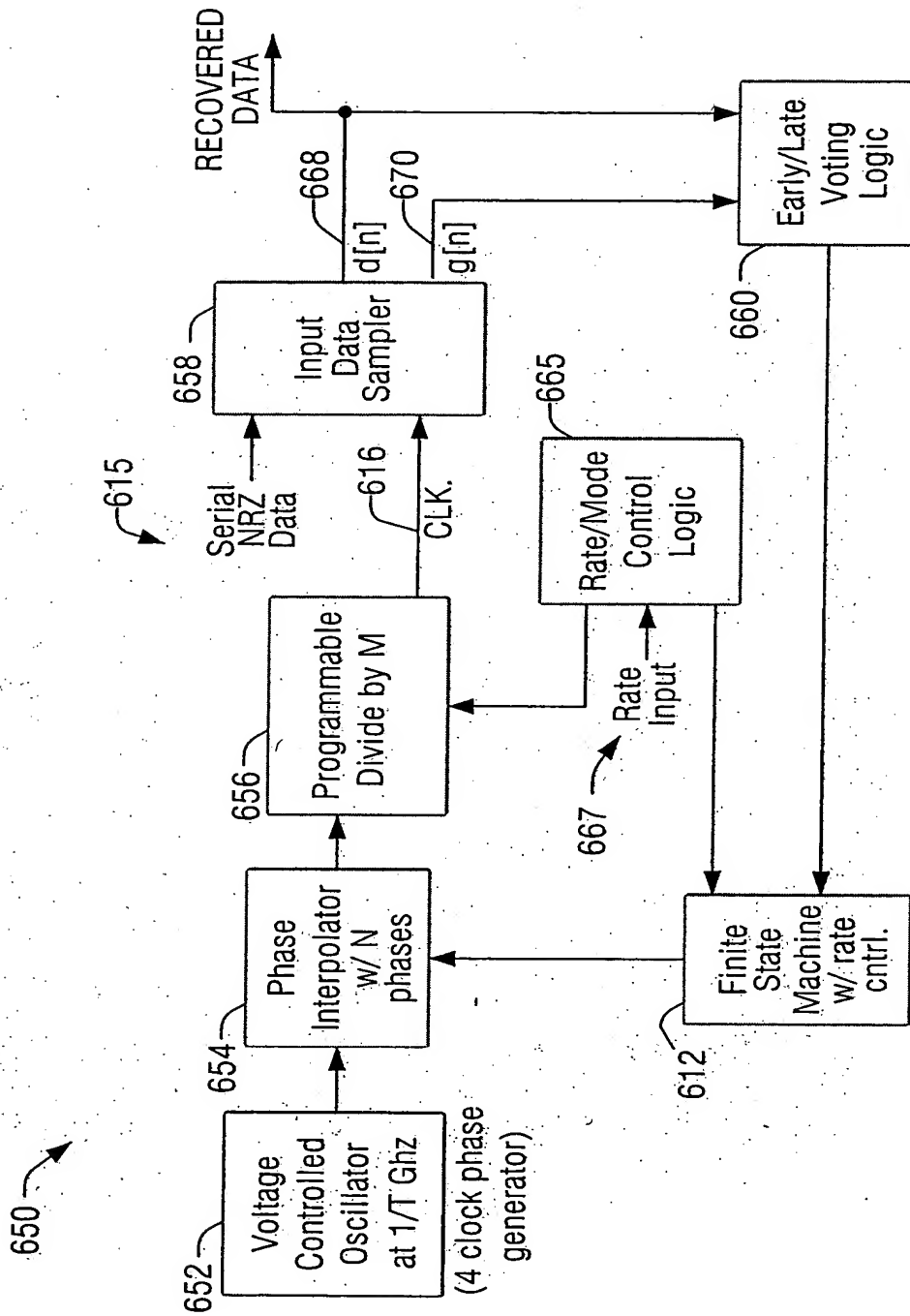


FIG. 6B

8/16

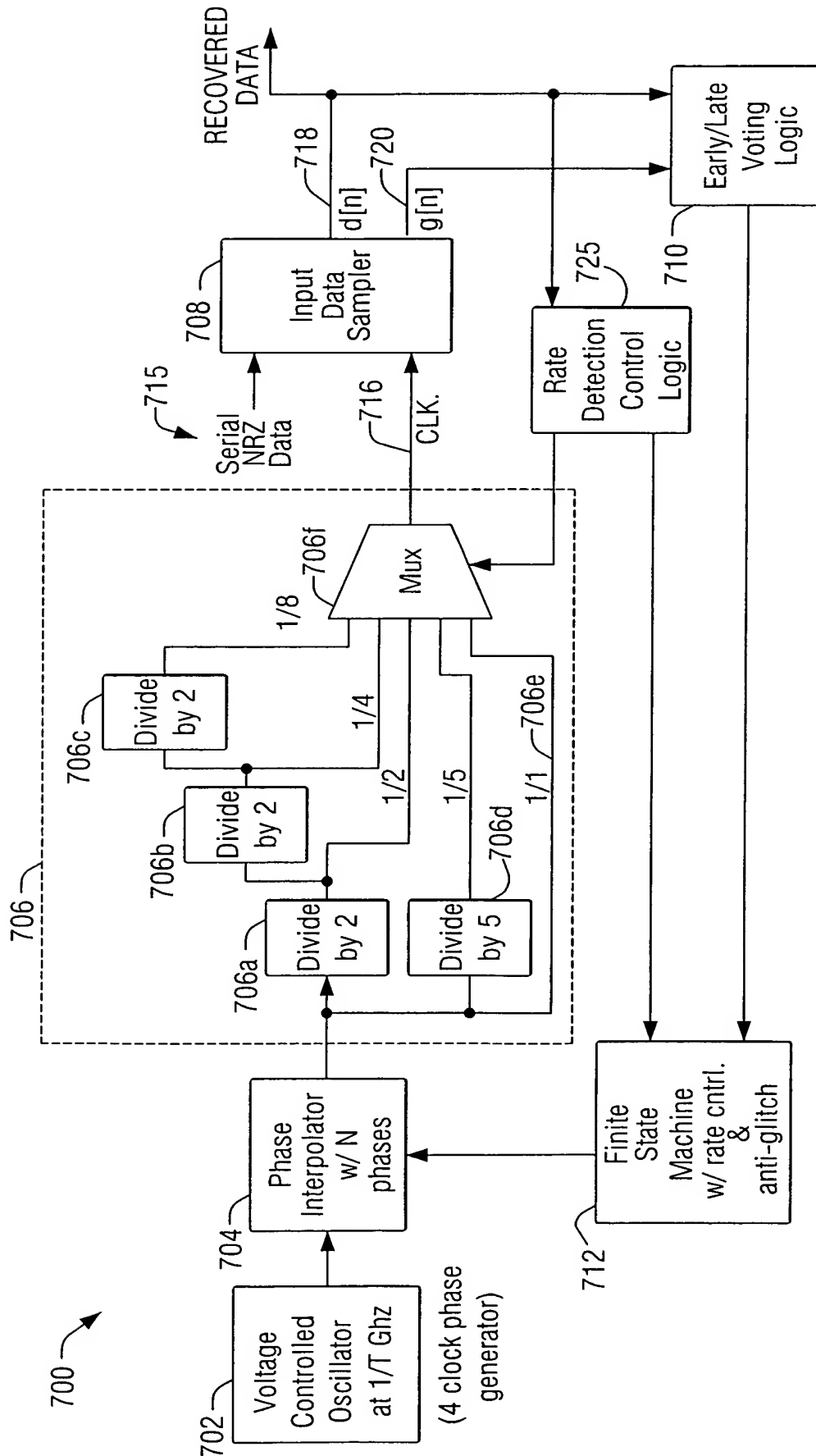


FIG. 7

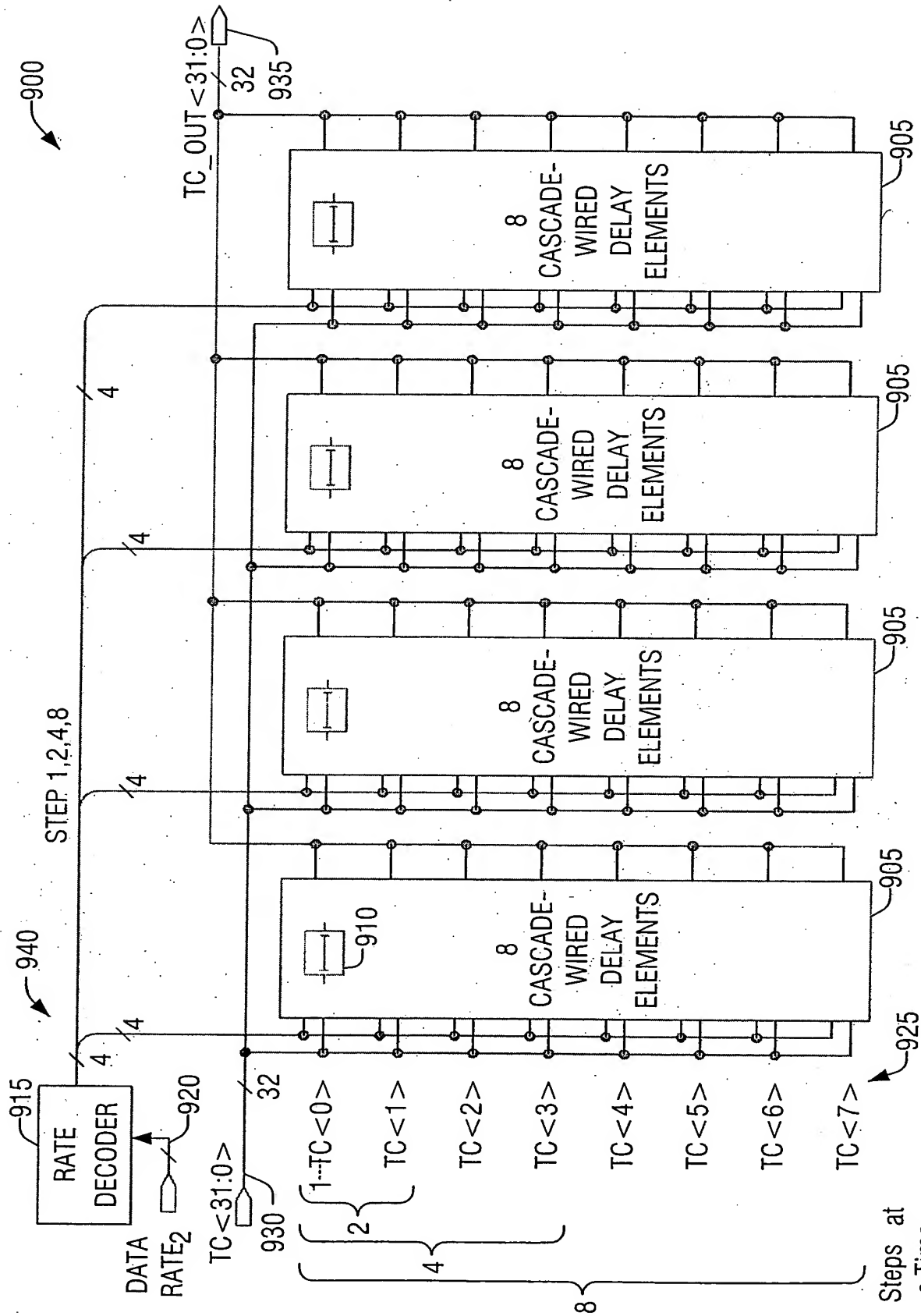
9/16

800

			Typical Implementation			Proposed Implementation		
Data Rate (Gbps)	Unit interval (ps)	Steps/ UI	Latency (bits)	Steps/ Update	Tracking ability (ppm)	Latency (bits)	Steps/ Update	Tracking ability (ppm)
12.5	80	64	32	1	488	32	1	488
6.25	160	128	32	1	244	32	2	488
3.125	320	256	32	1	122	32	4	488
1.5625	640	512	32	1	61	32	8	488
1.25	800	640	32	1	48.8	24	8	521

FIG.8

10/16



11/16

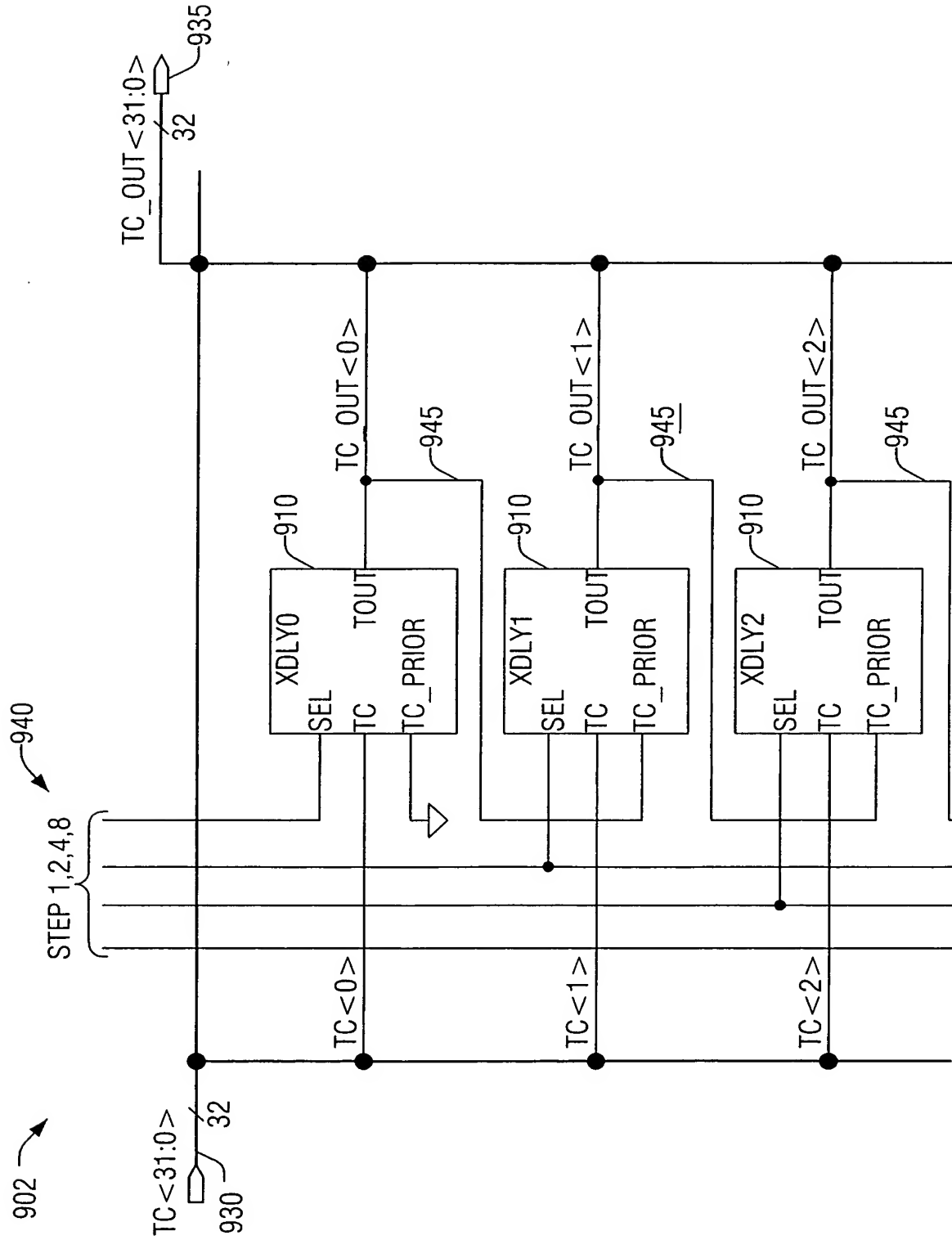


FIG. 9B

12/16

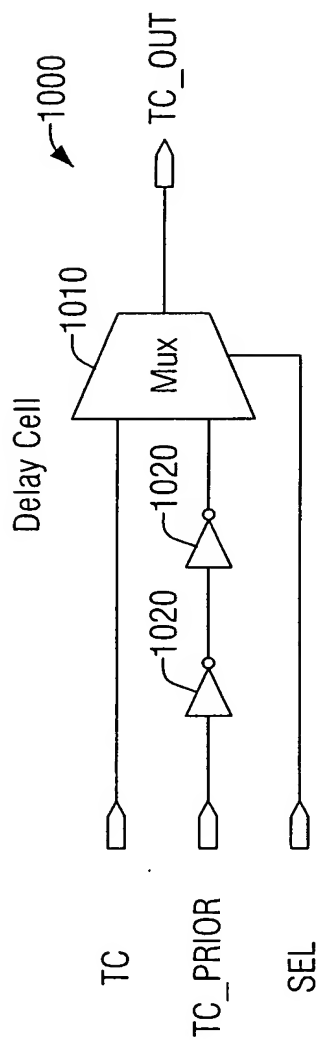


FIG. 10

TRANSIENT RESPONSE

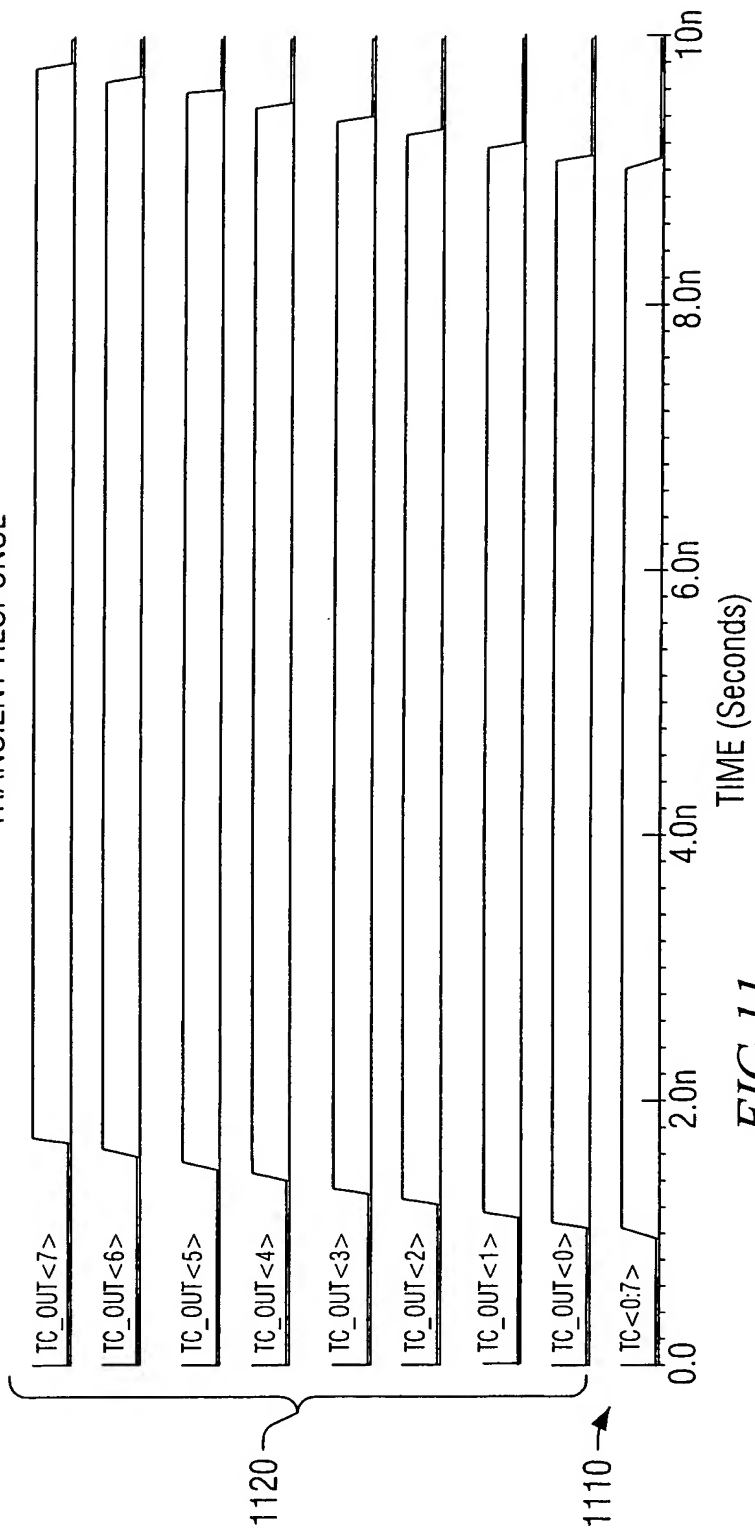
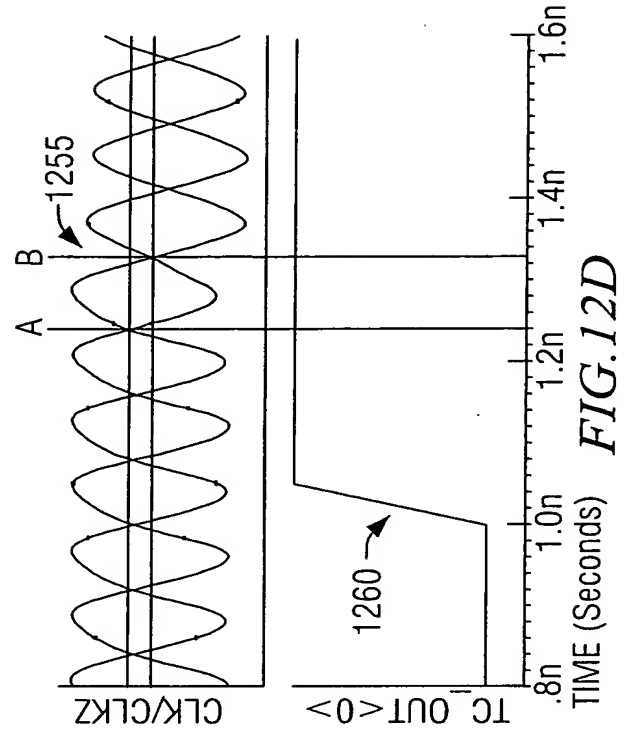
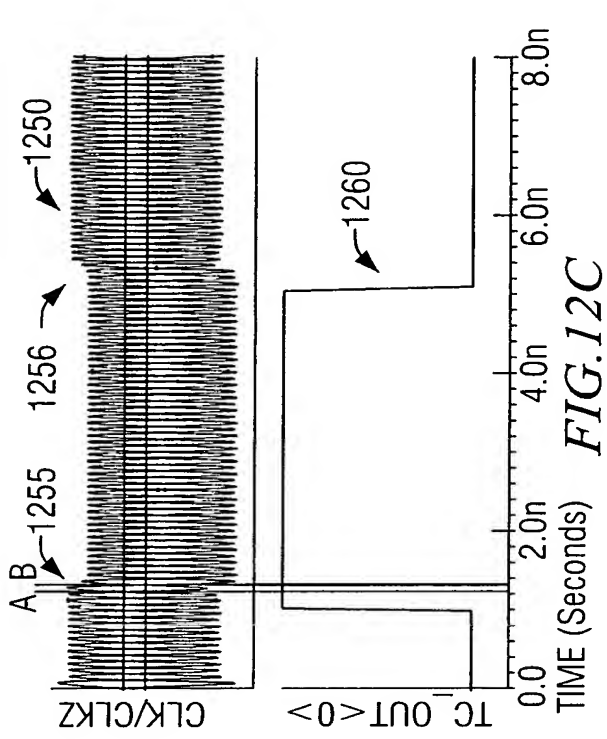
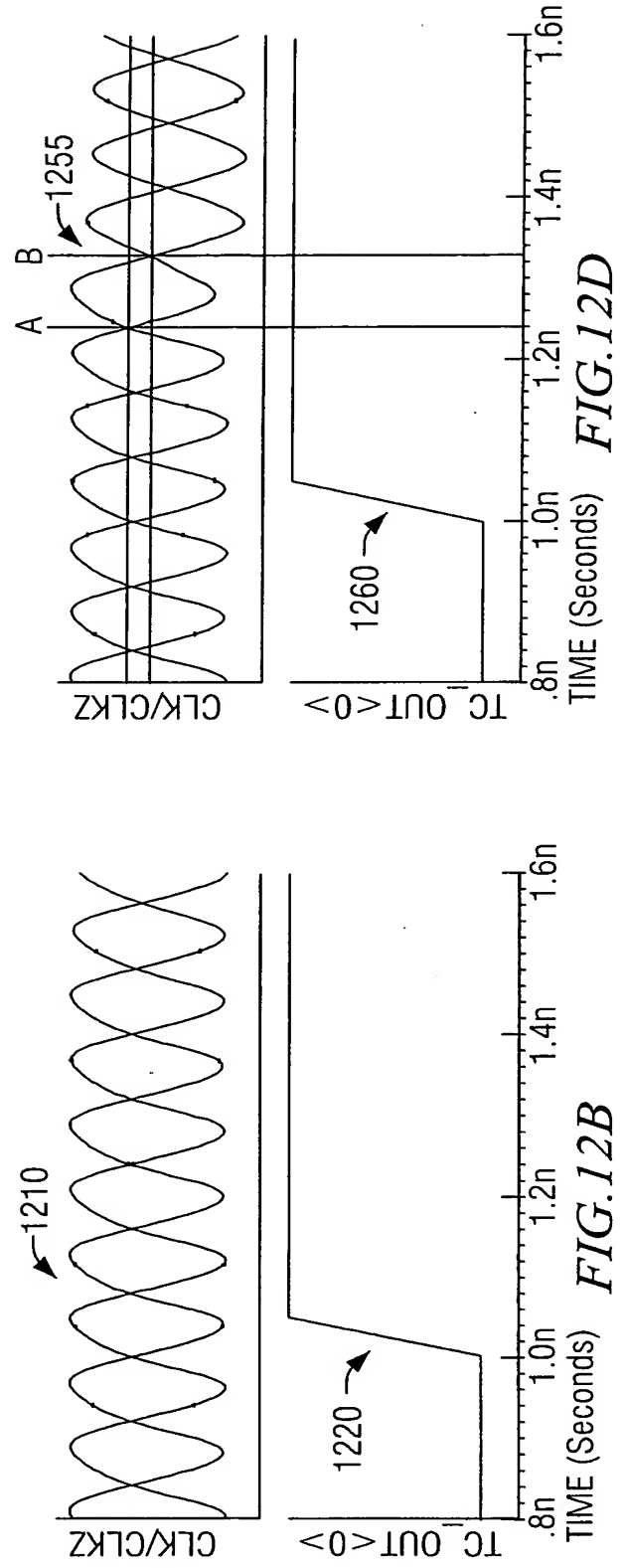
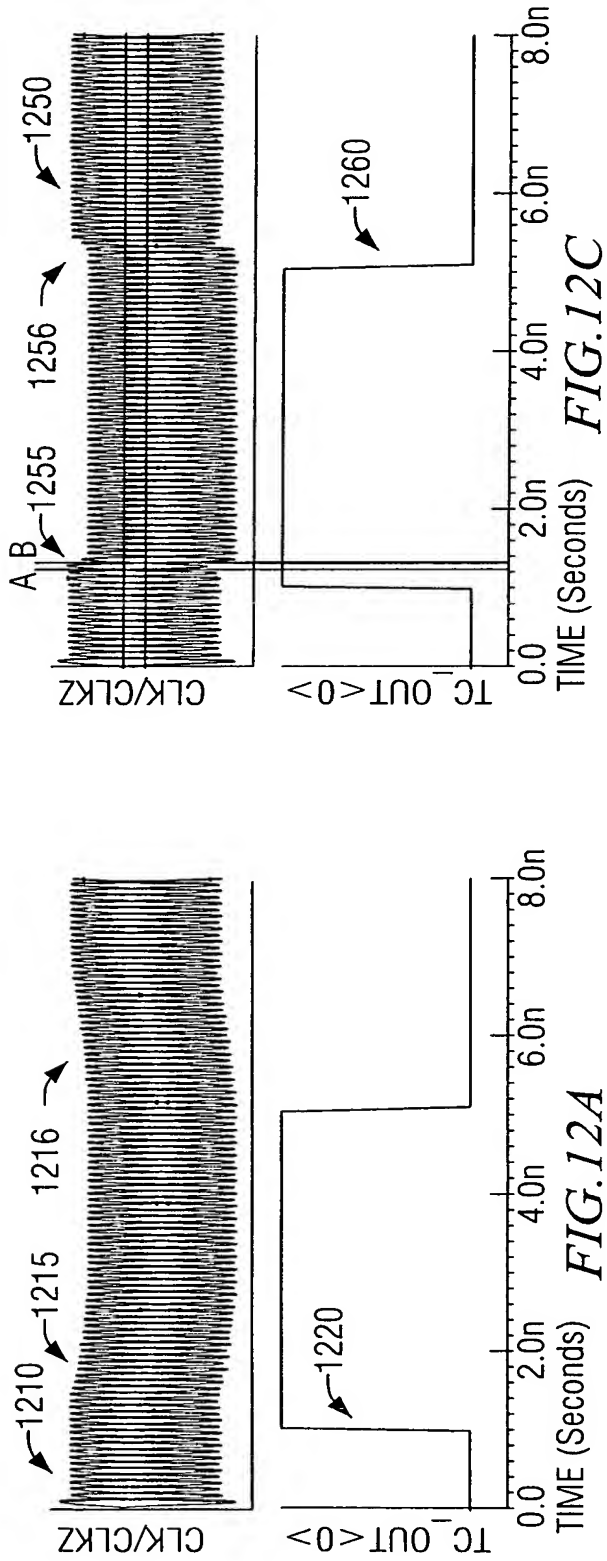


FIG. 11



14/16

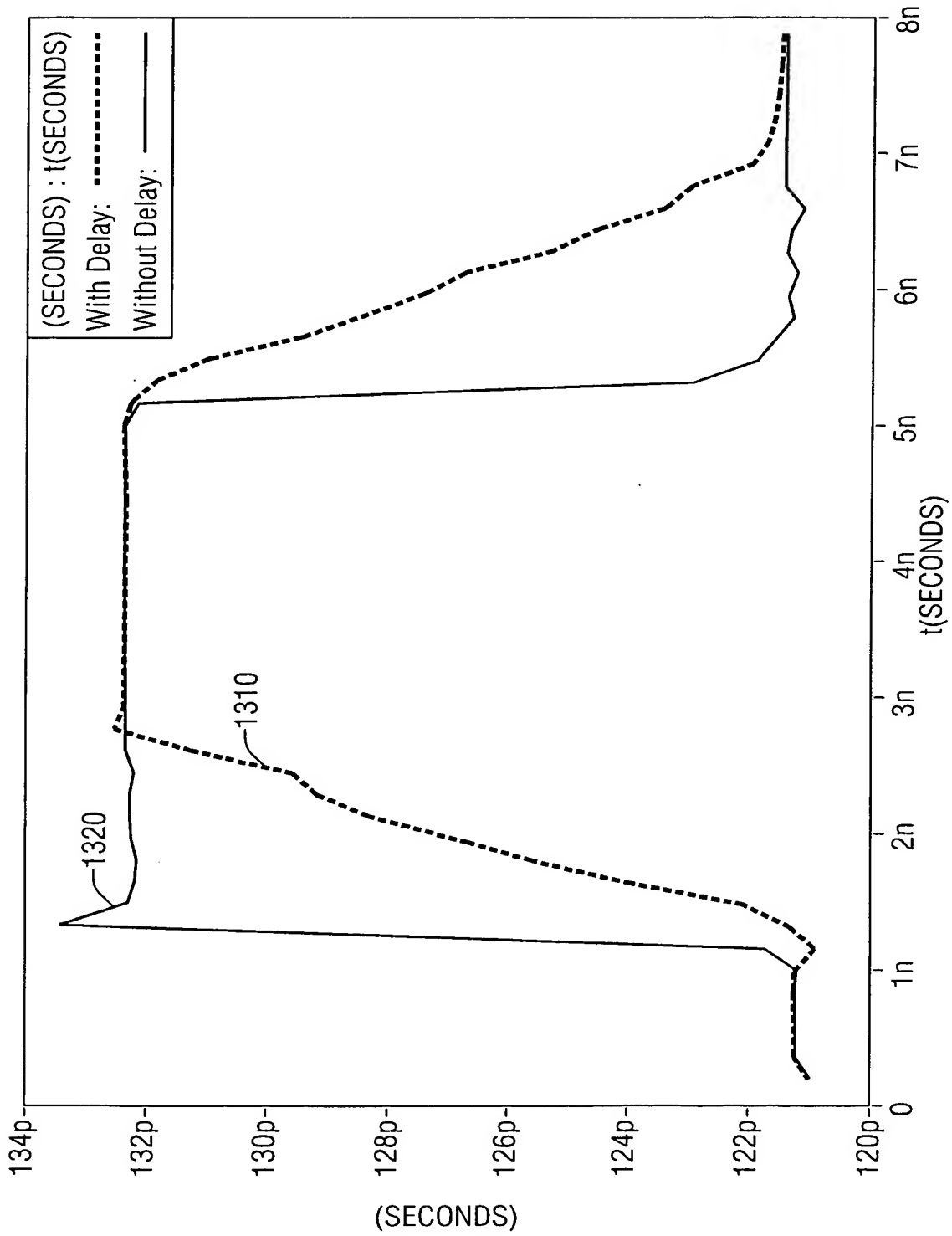


FIG. 13

15/16

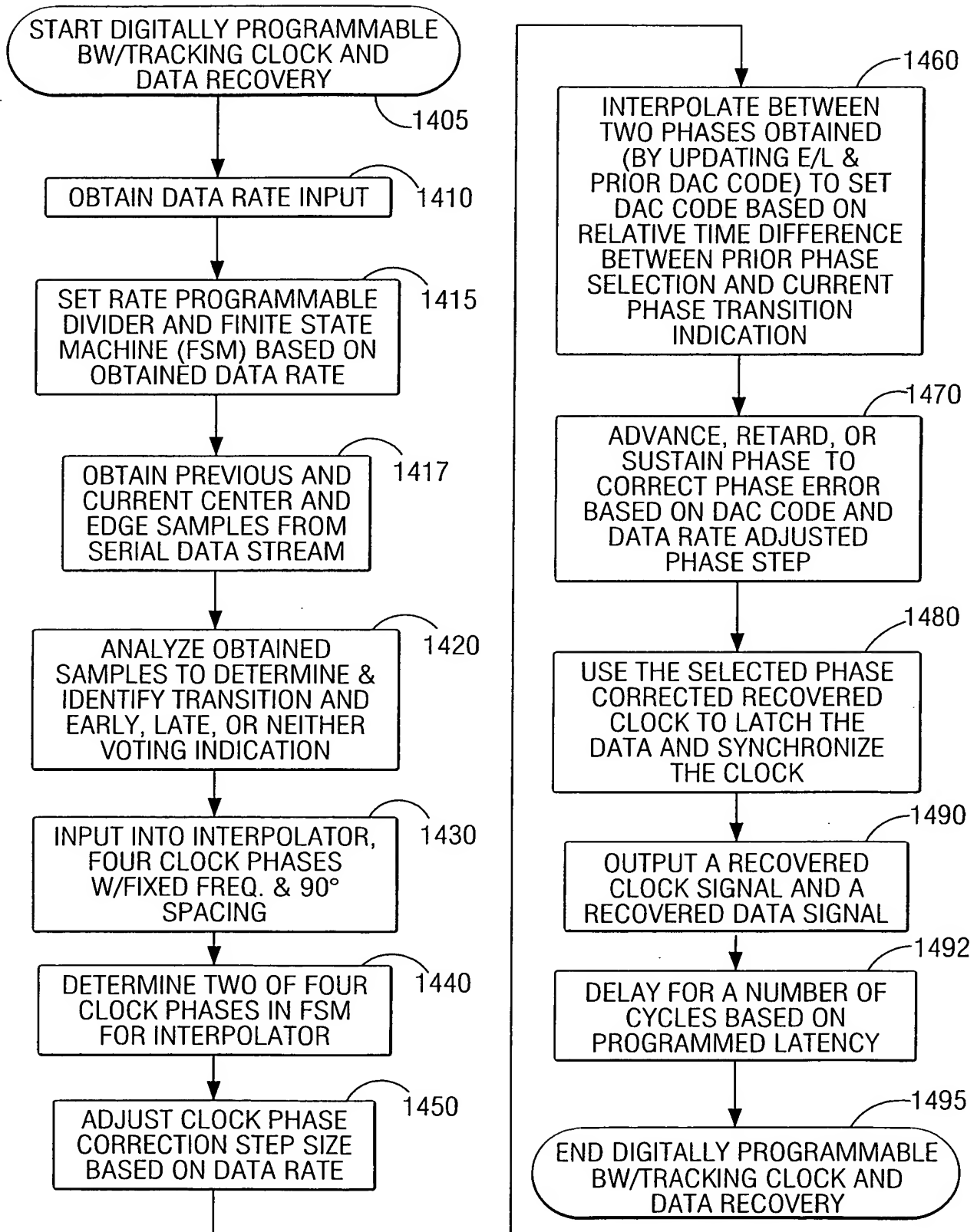


FIG. 14

16/16

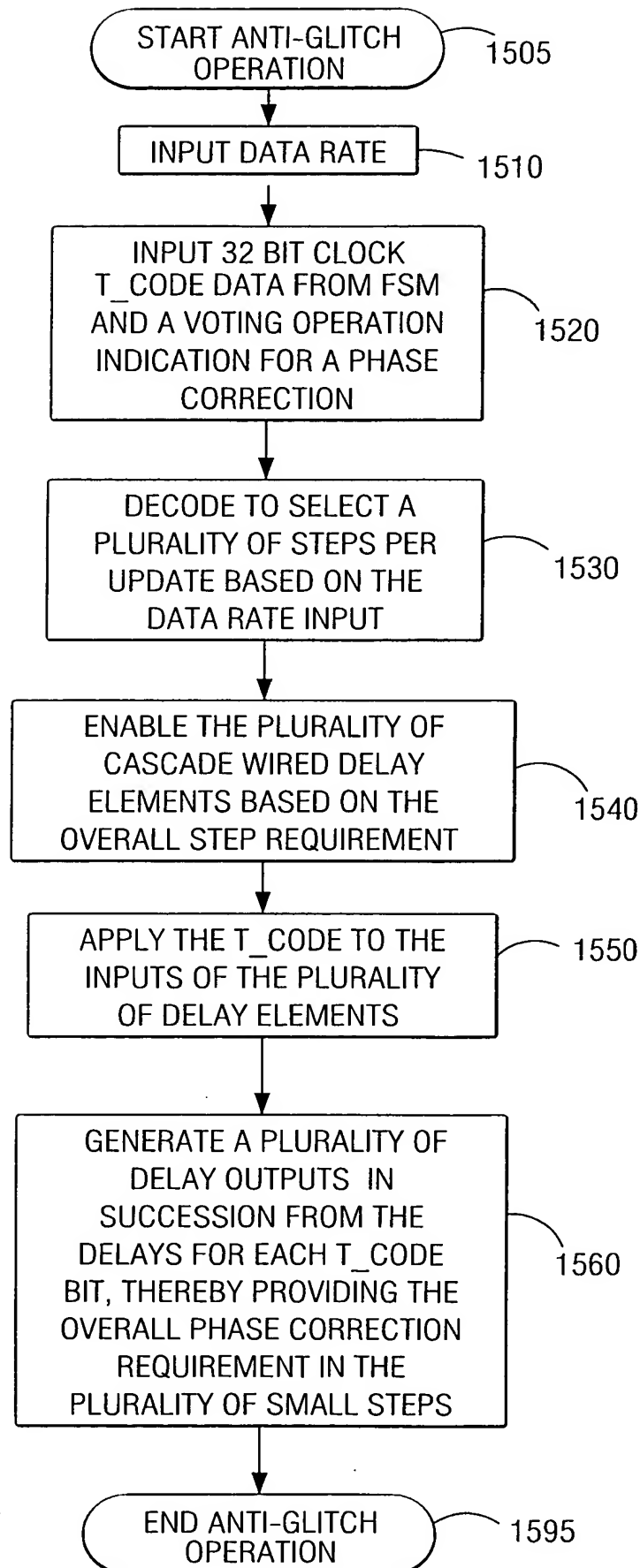


FIG. 15

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